Latency Measures in Network-on-Chips

(Bachelor-)/Masterthesis

Research field

In multiprocessor system-on-chips (MPSoCs), communication is usually built around an integrated network, a so-called network-on-chip (NoC). In order to assess the quality of a given NoC, various measures are used, such as the zero load latency (the time it takes to transfer packages through an empty network), the overall network latency and throughput for a given application, or the flit latency (the time it takes to process a single transfer unit (flit) after it is issued) for a random input pattern. While the flit latency is frequently used to derive the network's behavior under high pressure, this measure has inherent problems as its computation necessarily introduces a bias to the input data.

Research topic

The goal of the thesis is to systematically analyze the bias of the flit latency in different network topologies and to find other latency measures which avoid this bias. For the analysis, the SystemC NoC simulator *Ratatoskr* should be used.

Work plan

- Use Ratatoskr to generate heatmaps showing the data injection bias.
- Analyze the behavior of the measure for different examples and test this against other measures.
- Derive the advantages and disadvantages of the used latency measures.

Required skills

- Ability to systematically analyze a given problem
- Basic knowledge about Network-On-Chips (e.g. through lecture "System-On-Chip")
- (Basic) knowledge of Programming (preferably C/C++)

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