Design-Space Exploration for configurable Network-on-Chip in Mixed-Criticality Systems

Bachelor/Master Thesis/Research Project

Research field

Nowadays, with the developments of new Multi-Processor System-on-Chips (MPSoCs), the on-chip communication infrastructure is crucial for the performance of the system itself. These chips offer a heterogeneity of communication possibility, from simple direct link up to complex configurable Network-on-Chip (NoC) infrastructures[1]. NoCs are well explored in different aspects: topology, routing algorithm, streaming communications, isolation properties. Most of the works in literature, where a Design Space Exploration is conducted, consider the design of NoC itself starting from defining an optimal topology with the aim to build on the entire infrastructure for a target application. Yet, configurable NoCs are proposed in the new adaptive MPSoC (e.g., Versal programmable NoC), where a fixed physical infrastructure is already provided on the physical layer of the chip, and the topology or the routing algorithm are hidden to developers. New parameters, such as bandwidth required and class of priority must be provided to a "NoC compiler" for configuring the programmable NoC, allowing a fast and efficient utilisation. Configurable NoCs open new challenges, when the communication infrastructure must rely not only on performance but also on dependable requirements of Mixed-Criticality Systems (MCS), where different tasks and applications must share the same resources, without interfering each other. For these reasons, a framework that allows developers to simulate and analyse their application, from the communication prospective can be useful [2].

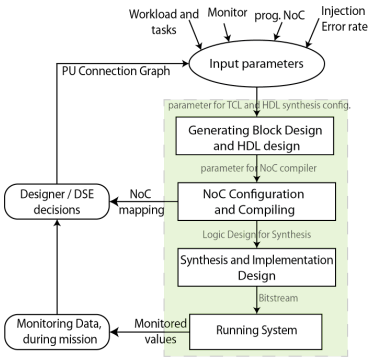

Figure 1: Tool flow for NoC

Research topic and working hypothesis

A Design Space Exploration process of a programmable NoC should be done, which consider Mixed-Criticality System (MCS) parameters. For doing it, a framework for on-chip simulation should be implemented. This framework gets different input parameters such as the tasks graph, the NoC and MCS parameters, as shown in Fig. 1. The framework generates the corresponding RTL design that must be synthesize for running on the device and monitoring errors events during the mission time. The aim is to provide a design framework where the designer can monitoring the network behavioural a priori. The student can focus his work on different aspects of the Design Space Exploration process and framework features, e.g., by implementing a traffic generator for dynamic workloads.

Work plan

- Study of the problem: NoC architecture and programmable NoC with related parameters and features.
- Definition of one or more features/parameters to include in the DSE with the simulator.
- Implementation of the proposed enhancement.
- Evaluation of the work done compared with the state-of-the-art.
- Success!

Required skills

- Knowledge in SoC and NoC.
- Possible Knowledge of one of these languages: C/C++, Pyton, HDL, TCL for Xilinx.

Contact

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References

[1] Ian Swarbrick, Dinesh Gaitonde, Sagheer Ahmad, Brian Gaide, and Ygal Arbel. 2019. Network-on-Chip Programmable Platform in Versal^{TM} ACAP Architecture. In Proceedings of the 2019 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA '19). Association for Computing Machinery, New York, NY, USA, 212–221. DOI:https://doi.org/10.1145/3289602.3293908

[2] Jan Moritz Joseph, Lennart Bamberg, Imad Hajjar, Behnam Razi Perjikolaei, Alberto García-Ortiz, and Thilo Pionteck. 2021. Ratatoskr: An Open-Source Framework for In-Depth Power, Performance, and Area Analysis and Optimization in 3D NoCs. ACM Trans. Model. Comput. Simul. 32, 1, Article 3 (January 2022), 21 pages. DOI:https://doi.org/10.1145/3472754